REMARKS/ARGUMENTS

The present application contains claims 1-4, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, 35 and 37-71. Claims 37-71 have been withdrawn from consideration as being directed to a non-elected invention. Claims 5 and 7 have been cancelled and their limitations have been added to claim 1, amended. Claims 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34 and 36 have been cancelled without prejudice to Applicant to expedite the prosecution of the present application.

It is noted that the present Action is non-final and that a three (3) month response period has been set to expire April 16, 2009. It is submitted that this Amendment has been timely filed.

Specification

The specification has been amended to cure certain minor informalities. No new matter has been added.

Drawings, Foreign Priority Claim and Priority Documents

It is noted that the drawings filed December 1, 2005 have been accepted; that the foreign priority claim has been acknowledged and that all of the priority documents have been received.

Claim Rejections - 35 U.S.C. §103

Making reference to the Detailed Action, claims 1-6 have been rejected under 35 U.S.C. §103(a) as unpatentable over John F. Bloomfield et al. (U.S. Patent Application Publication No. 2001/0036322) (hereinafter, "Bloomfield et al."). This rejection is respectfully traversed with regard to claims 1-4, claims 5 and 7 having

been cancelled and their limitations added to amended claim 1 and claim 6 having been cancelled to expedite the prosecution of the present application.

Although Bloomfield et al. makes reference to pipeline processing in the various paragraphs mentioned by the Examiner in the Office Action, the pipeline processing referred to paragraphs [0020], [0045], [0097], [0101] and [0109] is described in these paragraphs in very generalized terms.

Bloomfield et al. teaches that camera-captioned image data is converted from parallel data to serial data by sensor interface 22 and this serial data is then serially transmitted to modular image processing system (MIPS) 25 by way of the serial sensor link 24. Data is subsequently stored in image memory 34 and the image is processed by processing unit 38. Units 22, 24, 25 and 38 are shown in Fig. 2 of Bloomfield et al. The sensor interface 22 is described in paragraph [0058] as converting high speed parallel signals and serial signals. The serializer/deserializer 62 is described in paragraphs [0056] and [0059] as converting data into a serial stream. Eight (8) interfaces 110 are described in paragraph [0064] as converting serial data to parallel data.

However, none of these converters teach or even remotely suggest the first data-order converting unit of the present application which, as recited in amended claim 1, sequentially reads image data in units of a block row-by-row in the row direction from the memory. Note, for example, Fig. 7A of the present application in which data is read in blocks from frame memory 4 row-by-row in the horizontal direction and stored in memory 5a of the first data order converting unit 5. The order of the image data in block units thus read and obtained is unchanged and maintained as-is. In the next operation, the image data in block units is sequentially outputted column-by-column in the column direction. In the example given in Fig. 7A of the present application, in the write-in and read-out positions

shown in Fig. 7A, it should be understood that data was previously read out block-by-block from frame memory 4 into memory 5b. Frame memory 4 is then coupled to memory 5a to read the next group of blocks of data in the row-by-row manner in the horizontal direction into memory 5a, whereas the group of blocks previously read from frame memory 4 into memory 5b are read out to the image processing unit 6 block-by-block in the vertical direction in the column-by-column manner. The frame memory and the image processing unit continue to reverse connections between memories 5a and 5b.

The image data with the changed order is then image-processed by the image processing unit 6. The second data-order converting unit operates in a reverse manner from the first data-order converting unit. The second data-order converting unit outputs the image process image data changing its data order so as to be restored to that of the original image data.

Bloomfield et al. is limited to teaching simple parallel-serial conversion and serial-parallel conversion and neither teaches nor remotely suggests any change in the reading or writing order of image data when storing converted image data to image memory 34 or when processing unit 38 conducts image processing. In addition, there is clearly no teaching of restoring the image data to the original data order since Bloomfield et al. fails to teach changing the data order from its original order.

Claim 1, as amended, positively recites all of the above limitations and it is submitted that claim 1 patentably distinguishes over Bloomfield et al. Claims 2-4 all depend from claim 1 and carry all of its limitations and hence are deemed to patentably distinguish over Bloomfield et al. for the same reasons set forth above regarding claim 1.

Claims 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33 and 35 all depend from claim 1 or from a claim which depends from claim 1 and are likewise submitted to patentably distinguish over Bloomfield et al.

Claims 7 and 8 have been rejected under 35 U.S.C. §103(a) as unpatentable over Bloomfield et al. in view of Kozo Akiyoshi et al. (U.S. Patent Application Publication No. 2002/0126917) (hereinafter, "Akiyoshi et al."). Claim 8 having been cancelled without prejudice to Applicant to expedite the prosecution of the present application, this rejection is moot as regards to claim 8. It should be noted that the limitations of claim 7 have been added to claim 1 and it is submitted that amended claim 1, which incorporates the limitations of claim 7, patentably distinguishes over Bloomfield et al. in the sense of 35 U.S.C. §103 as well as 35 U.S.C. §102.

Even assuming, for the sake of argument that Akiyoshi et al. is combinable with Bloomfield et al. to incorporate the limitations relating to distortion correction and processing, it is submitted that Akiyoshi et al. is lacking in the same teachings lacking in Bloomfield et al. as pointed out above and it is submitted that claim 1, which incorporates the limitations of claim 7, patentably distinguishes over Bloomfield et al. either alone or in combination with Akiyoshi et al. and it is submitted that claim 1 patentably distinguishes thereover as well as claims 2-4, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33 and 35.

Conclusion

If the Examiner believes that any additional minor formal matters need to be addressed in order to place this application in condition for allowance, or that a telephone interview will help to materially advance the prosecution of this application, the Examiner is invited to contact the undersigned by telephone at the Examiner's convenience.

In view of the foregoing amendment and remarks, Applicants respectfully submit that the present application, including claims 1-4, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, and 35, is in condition for allowance and a notice to that effect is respectfully requested.

Respectfully submitted,

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